

- 1 1. A coprocessor interface between a central processing  
2 unit (CPU) and a coprocessor, the interface  
3 comprising:  
4 an instruction transfer signal group for transferring  
5 a plurality of instruction types from the CPU to  
6 the coprocessor; and  
7 a busy signal group, coupled to said instruction  
8 transfer signal group, for signaling said  
9 instruction transfer signal group when one or  
10 more of said plurality of instruction types  
11 cannot be transferred;  
12 wherein when said instruction transfer signal group  
13 receives said signaling for one or more of said  
14 plurality of instruction types, said instruction  
15 transfer signal group does not transfer those  
16 instruction types, but transfers other ones of  
17 said plurality of instruction types.
- 1 2. The coprocessor interface as recited in claim 1  
2 wherein the coprocessor comprises:  
3 A Floating-Point Coprocessor; or  
4 A 3-D Graphics Accelerator.

1 3. The coprocessor interface as recited in claim 1  
2 wherein said plurality of instruction types comprise:  
3 arithmetic instructions; and  
4 data transfer instructions.

1 4. The coprocessor interface as recited in claim 3  
2 wherein said data transfer instructions comprise:  
3 TO Coprocessor data transfer instructions; and  
4 FROM Coprocessor data transfer instructions.

1 5. The coprocessor interface as recited in claim 1  
2 wherein said instruction transfer signal group  
3 comprises:  
4 an instruction signal group, for carrying said  
5 plurality of instruction types from the CPU to  
6 the coprocessor; and  
7 a plurality of strobe signals, each associated with a  
8 different one of said plurality of instruction  
9 types.

1 6. The coprocessor interface as recited in claim 5  
2 wherein when one of said plurality of instruction  
3 types is dispatched on said instruction signal group,  
4 its transfer is completed by assertion of an  
5 associated one of said plurality of strobe signals.

1 7. The coprocessor interface as recited in claim 1  
2 wherein said busy signal group comprises:

3 an arithmetic busy signal; and

4 a data transfer busy signal group.

1 8. The coprocessor interface as recited in claim 7  
2 wherein said data transfer busy signal group  
3 comprises:

4 a TO Coprocessor data transfer busy signal; and

5 a FROM Coprocessor data transfer busy signal.

1 9. The coprocessor interface as recited in claim 1  
2 wherein when said busy signal group stops signaling  
3 said instruction transfer group that said one or more  
4 of said plurality of instruction types cannot be  
5 transferred, said instruction transfer group begins  
6 transfer of those instruction types, if necessary.

1 10. The coprocessor interface as recited in claim 1  
2 wherein said instruction transfer signal group  
3 transfers two or more of said plurality of instruction  
4 types from the CPU to the coprocessor, in parallel.

1 11. The coprocessor interface as recited in claim 10  
2 further comprising:

3 an instruction order signal group, coupled to said  
 4 instruction transfer signal group, for indicating  
 5 to the coprocessor a relative execution order for  
 6 said two or more of said plurality of instruction  
 7 types that are transferred in parallel.

1 12. The coprocessor interface as recited in claim 11  
 2 wherein said two or more of said plurality of  
 3 instruction types that are transferred in parallel  
 4 comprise:

5 an arithmetic instruction; and  
 6 a data transfer instruction.

1 13. A computer program product for use with a computing  
 2 device, the computer program product comprising:

3 a computer usable medium, having computer readable  
 4 program code embodied in said medium, for causing  
 5 a coprocessor interface to be described, said  
 6 computer readable program code comprising:

7 first program code for providing an instruction  
 8 transfer signal group for transferring a  
 9 plurality of instruction types from a CPU to  
 10 a coprocessor; and

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11 second program code for providing a busy signal  
 12 group for signaling said instruction  
 13 transfer signal group when one or more of  
 14 said plurality of instruction types cannot  
 15 be transferred.

14. The computer program product group, as recited in  
 claim 13 wherein when said instruction transfer signal  
 group receives said signaling for one or more of said  
 plurality of instruction types, said instruction  
 transfer signal group does not transfer those  
 instruction types, but transfers other ones of said  
 plurality of instruction types.

14. The computer program product group, as recited in  
 claim 13 wherein said instruction transfer signal  
 group comprises:  
 an instruction signal group, for carrying said  
 plurality of instruction types from the CPU to  
 the coprocessor; and  
 a plurality of strobe signals, each associated with a  
 different one of said plurality of instruction  
 types.

15. A computer data signal embodied in a transmission  
 medium comprising:

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3 computer-readable first program code for providing an  
 4 instruction transfer signal group for  
 5 transferring a plurality of instruction types  
 6 from a CPU to a coprocessor; and

7 computer-readable second program code for providing a  
 8 busy signal group for signaling said instruction  
 9 transfer signal group when one or more of said  
 10 plurality of instruction types cannot be  
 11 transferred;

12 wherein when said instruction transfer signal group  
 13 receives said signaling for one or more of said  
 14 plurality of instruction types, said instruction  
 15 transfer signal group does not transfer those  
 16 instruction types, but transfers other ones of  
 17 said plurality of instruction types.

1 <sup>16</sup>/<sub>17</sub>. The computer data signal as recited in claim <sup>15</sup>/<sub>16</sub>  
 2 wherein said instruction transfer signal group  
 3 transfers two or more of said plurality of instruction  
 4 types from the CPU to the coprocessor, in parallel.

1 <sup>17</sup>/<sub>18</sub>. The computer data signal as recited in claim <sup>16</sup>/<sub>17</sub>  
 2 further comprising:

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computer readable third program code for providing an instruction order signal group, coupled to said instruction transfer signal group, for indicating to the coprocessor a relative execution order for said two or more of said plurality of instruction types that are transferred in parallel.

19. An interface between a central processing unit (CPU) and a coprocessor for transferring data from the CPU to the coprocessor, wherein the data is transferred out-of-order with respect to its associated instructions, the interface comprising:

- a data instruction signal group, for transferring first and second data instructions from the CPU to the coprocessor;
- a data signal group, coupled to said data instruction signal group, for transferring first and second data, associated with said first and second data instructions, respectively, from the CPU to the coprocessor, out-of-order; and
- a data order signal group, coupled to said data group, for indicating to the coprocessor a relative data order of transfer for said first and second data.

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1 20. The interface as recited in claim 19 wherein said  
2 first and second data is transferred to the  
3 coprocessor without any tag information which would  
4 otherwise relate said first and second data with its  
5 (their) associated first and second data instructions.

1 21. The interface as recited in claim 19 wherein said data  
2 signal group comprises:

3 data signals, for dispatching said first and second  
4 data from the CPU; and

5 a TO coprocessor data strobe, coupled to said data  
6 signals, for signaling transfer of said first and  
7 second data to the coprocessor.

1 22. The interface as recited in claim 19 wherein said data  
2 order signal group comprises:

3 a data order signal line, for signaling to the  
4 coprocessor two distinct relative data orders for  
5 said first and second data, at the time said  
6 first and second data is transferred.

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1 23. An out-of-order data transfer interface between a  
2 central processing unit (CPU) and a coprocessor,  
3 comprising:

4 a data instruction signal group, for transferring M  
5 data instructions from the CPU to the  
6 coprocessor;

7 a data signal group, coupled to said data instruction  
8 signal group, for transferring M sets of data  
9 from the CPU to the coprocessor; and

10 a data order signal group, coupled to said data signal  
11 group, said data order signal group having  $2^N$   
12 distinct signals, for indicating to the  
13 coprocessor, for each of said M sets of data that  
14 are transferred, their relative order of transfer  
15 with respect to said M data instructions.

1 24. The out-of-order data transfer interface as recited in  
2 claim 23 wherein said data order signal group  
3 comprises three ( $N=3$ ) distinct signals, for indicating  
4 a relative order of transfer for up to 8 outstanding  
5 ones of said M sets of data.

1 25. The out-of-order data transfer interface as recited in  
2 claim 23 further comprising:

3 an order limit signal group, coupled to said data  
4 signal group, for signaling a relative data order  
5 limit of the coprocessor to the CPU;

6 wherein when the CPU receives signaling from said  
7 order limit signal group, said data signal group,  
8 will not exceed said relative data order limit  
9 when transferring said M sets of data.

1 26. The out-of-order data transfer interface as recited in  
2 claim 23 wherein said data instruction signal group  
3 also transfers M data instructions from the  
4 coprocessor to the CPU, said data signal group also  
5 transfers M sets of data from the coprocessor to the  
6 CPU; and said data order signal group also indicates  
7 to the CPU, the relative order of transfer of said M  
8 sets of data from the coprocessor with respect to  
9 their said M data instructions.

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1 27. A coprocessor interface for establishing instruction,  
2 data, and control communication between a central  
3 processing unit (CPU) and a coprocessor, the interface  
4 providing for coprocessor evaluation of CPU  
5 conditional instructions, the interface comprising:

6 an instruction transfer group for providing the CPU  
7 conditional instructions to the coprocessor; and  
8 a condition code check signal group, coupled to said  
9 instruction transfer group, for transferring  
10 condition code checkss from the coprocessor to  
11 the CPU upon evaluation of the CPU conditional  
12 instructions by the coprocessor.

1 28. The coprocessor interface as recited in claim 27  
2 wherein the CPU, upon receipt of said condition code  
3 checks from the coprocessor, either executes, or does  
4 not execute, the CPU conditional instructions, based  
5 on the value of said condition code checks.

1 29. The coprocessor interface as recited in claim 27  
2 wherein said condition code checks signal the CPU to  
3 either execute, or not execute, the CPU conditional  
4 instructions.

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- 1 30. A method for transferring instructions, and data  
2 associated with the instructions, from a central  
3 processing unit (CPU) to a coprocessor, where the data  
4 associated with the instructions is transferred in  
5 variable time slots after transfer of their associated  
6 instructions, and out-of-order with respect to their  
7 associated instructions, the method comprising:  
8 transferring the instructions to the coprocessor;  
9 tracking the number of outstanding instructions that  
10 require data for execution; and  
11 providing, along with each data transfer, a relative  
12 order indication, to associate each data transfer  
13 with one of the number of outstanding  
14 instructions that require data for execution;  
15 wherein the coprocessor utilizes the relative order  
16 indication to place each data transfer with its  
17 associated instruction.
- 1 31. The method as recited in claim 30 wherein the  
2 coprocessor monitors outstanding instructions that  
3 require data for execution from oldest to youngest,  
4 and updates the relative order of outstanding  
5 instructions upon receipt of each data transfer.